9. The thin-film transistor array panel of claim 1, wherein the second gate electrode overlaps the first gate electrode.

10. The thin-film transistor array panel of claim 1, further comprising:

an etching stop layer overlapping the semiconductor between the source electrode and the drain electrode.

11. A method of forming a thin-film transistor array panel, the method comprising:

forming a first gate electrode on a substrate;

forming a first self-assembled monolayer on the first gate electrode;

forming a gate insulating layer on the first self-assembled monolayer;

forming a semiconductor on the gate insulating layer;

forming a drain electrode overlapping the semiconductor, the drain electrode being separated from and facing a source electrode with respect to the semiconductor;

forming a first interlayer insulating layer on the source electrode and the drain electrode;

forming a second self-assembled monolayer on the first interlayer insulating layer;

forming a second gate electrode on the second self-assembled monolayer;

forming a second interlayer insulating layer on the second gate electrode; and

forming a pixel electrode on the second interlayer insulating layer and connected to the drain electrode.

12. The method of claim 11, wherein:

the first self-assembled monolayer comprises a first polymer material comprising a thiol group; and

the second self-assembled monolayer comprises a second polymer material comprising a silane group.

13. The method of claim 12, wherein:

the semiconductor is doped with N-type conductivity impurities;

the first self-assembled monolayer comprises a fluoroaryl thiol derivative; and

the second self-assembled monolayer comprises a fluoroaryl silane derivative or a fluoroalkyl silane derivative.

14. The method of claim 12, wherein:

the semiconductor is doped with P-type conductivity impurities;

the first self-assembled monolayer comprises an aminoaryl thiol derivative; and

the second self-assembled monolayer comprises an aminoalkyl silane derivative or an aminoaryl silane derivative.

15. The method of claim 11, wherein forming the first self-assembled monolayer comprises removing a portion of the first self-assembled monolayer by cleansing, such that the first self-assembled monolayer covers the first gate electrode.

16. The method of claim 15, wherein forming the second self-assembled monolayer comprises etching a portion of the second self-assembled monolayer, such that the second self-assembled monolayer overlaps the second gate electrode.

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